# The Chemistry of the Semiconductor Industry

**Sean C. O'Brien**
*Semiconductor Process and Device Center, Texas Instruments, PO Box 655012 MS 944, Dallas TX 75265, USA; email: sobrien @spdc.ti.com*

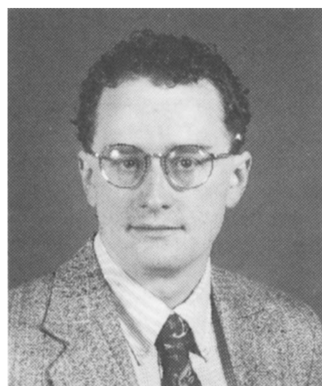
The explosive growth of the semiconductor industry can be directly related to inexpensive ultraclean chemical processing which leads to highly controlled films and surfaces. Areas of semiconductor wafer processing which involve chemical reactions include silicon crystal growth, high temperature oxidations, chemical vapour deposition, and photochemical reactions in lithographic resist masks. This article will concentrate on the field of contamination and film removal using liquid and gas phase chemical reactions. This area more than any other is in desperate need of fundamental chemical study to determine reaction kinetics, and mechanisms.

## 1 Semiconductor Wafer Processing

The starting point in chip manufacturing is silicon wafers which are nearly perfect crystals cut *ca.* 1 mm thick with a precise crystal axis orientation and then polished to an rms flatness less than 800 nm depth per cm of length. All new semiconductor manufacturing facilities are being built to utilize 200 mm diameter wafers, thus hundreds of working chips can be constructed on every wafer. Initial plans are being laid for the conversion to 300 mm wafers. In general, the cost to produce a wafer does not drastically depend on the diameter, yet the total number of chips which can be made on a wafer depends directly on the available area. Thus, the bigger the wafer the less the cost per chip.

Wafer fabrication facilities are commonly known as wafer fabs, and typically this means a cleanroom. This is a room with a ceiling filled with filtered fans which blow ultraclean air downwards. The air is supposed to experience laminar flow, then exit the room through the floor. A modern Class 1 cleanroom has approximately a single particle (greater than 0.1 μm diameter) per cubic metre of air space. This room is many orders of magnitude cleaner than the best hospital operating room. Workers are enclosed in clean suits, the newest versions of which now allow no exposed skin or hair. This environment accounts for a small fraction of the total money spent on chip manufacturing; wafer processing tools require nearly 90% of the cost.

On the wafer surface an $SiO_2$ film is nearly universally called oxide, it is used as an insulator, and as the active gate in a transistor. There are a wide variety of oxide films; they vary with chemical vapour deposition (CVD) or oxidation parameters, doping levels, and high temperature thermal processing. The difference between deposited and grown oxide films is the source of silicon; CVD films get the silicon from gaseous precursors, while direct reaction between oxygen and the crystal silicon leads to grown films. $Si_3N_4$ (routinely known as nitride) gives a dense insulating film used for certain lithographic steps, as a permanent dielectric film, and as a barrier to contaminants. CVD silicon is widely used as a conducting film early in the chip manufacture where metallic lines would severely contaminate the wafer. CVD silicon is usually called polysilicon (or simply poly) while the term amorphous silicon is also used. The difference between poly and amorphous silicon is in the grain structure of the film.



*Sean O'Brien received a BS in Chemistry from the University of Illinois in 1984. He received a PhD in chemistry from Rice University in 1988 for work on the discovery and photophysics of $C_{60}$. His postdoctoral research at Rice focused on femtosecond dissociation dynamics using Raman spectroscopy. He joined Texas Instruments in 1990 and currently works on surface preparation of wafers with exposed metal films for advanced CMOS device technology.*

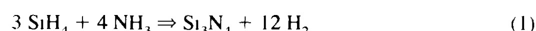
From the first moment when pure crystal silicon is produced for wafer production, until the final polymer coating is applied to hermetically seal a working chip, the manufacturing of semiconductors is dominated by chemical reactions.[1] The various segments of the production process can be loosely separated into wafer manufacturing, thermal processing, thin film deposition, lithographic pattern definition, chemical mechanical planarization, anisotropic pattern etching, and contamination removal/surface preparation.[2] Many processes cross these boundaries, so these labels should only be used conceptually.

Silicon wafer manufacturing consists of obtaining ultrapure silicon, melting it down, further purification, adding precisely controlled amounts of dopants (such as B), then crystallizing the liquid from a spinning apparatus into a boule up to 300 mm in diameter over 1 metre long. Eliminating all impurities is critical for ultrafast transistor speeds. Iron contamination above $10^{10}$ atoms per $cm^3$ is unacceptable, oxygen above 30 ppm degrades device functionality.

The required characteristics of a good film for semiconductors are extreme, which explains why it is so rare for a new film to make the transition from research to manufacturing. These films must stick to the underlying surface, and must allow subsequent films to stick tightly. They must be very clean; impurities in precursors can easily poison the transistors. They must have tightly controlled deposition rates, with thickness non-uniformity near 2%. They must have a sharp distribution of electrical properties, such as the relative permitivity. Some films are required to fill gaps (as a liquid flows into crevices) while others must be completely conformal. Their resistance to semiconductor processing must be high, temperatures in excess of 800 °C and highly reactive plasma ion environments are common. Their precursors and waste product species must not be on any target environmental reduction lists. And finally they must cost a reasonable amount of money. It is a wonder that any films were ever found which could meet these requirements.

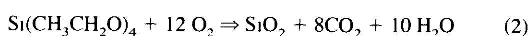
Thermal processing involves high temperature reactions, frequently with oxygen as a reactant. Growth of transistor dielectric films occurs as high as 1050 °C; growth of electrically insulating films occurs at even higher temperatures with $H_2O$ as a reactant. Finally, once dopants are implanted into precise regions a high temperature anneal will allow them to diffuse to their final location within the silicon.

CVD involves chemical reactions between gas phase precursors leading to growth on the surface of macroscopic films.[3] Silicon nitride is deposited as an insulating film using the chemical reaction (1).



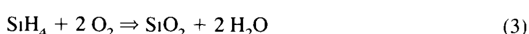
$$3\,SiH_4 + 4\,NH_3 \Rightarrow Si_3N_4 + 12\,H_2 \qquad (1)$$

Silicon dioxide is deposited using tetraethylorthosilicate (TEOS) in reaction (2),



$$Si(CH_3CH_2O)_4 + 12\,O_2 \Rightarrow SiO_2 + 8CO_2 + 10\,H_2O \qquad (2)$$

or from a silane precursor, eqn (3)



$$SiH_4 + 2\,O_2 \Rightarrow SiO_2 + 2\,H_2O \qquad (3)$$

Understanding the microscopic chemical reactions involved in these CVD processes is critical to maintaining optimized processing Uncontrolled deposition rates or initiation times can lead to non-uniform films of poor quality which lead to failed electrical devices The difference between conformal and gap-filling deposition frequently determines whether or not a film can be used The type of chemical study required is exemplified in a recent presentation by Takahashi *et al* [4] In this work they wrote down over 150 chemical reactions, took all the rate constants and plugged everything into a powerful computer analysis routine The result was a significant advancement in the understanding of CVD oxide properties using $SiH_4$ precursors in reaction (3) Silane oxide deposition with gap filling properties would be a fantastic addition to device processing, because it occurs several hundred degrees Celsius lower than TEOS deposition This would allow low-temperature dielectric film deposition, the 'holy-grail' of backend processing (backend means after metal lines have been added to the wafer) Prior to this work it was assumed that conformal deposition was the only result of silane deposition This is exactly the type of chemical research which can dramatically change the face of the industry

Photolithography is the technique which allows generation of millions of ultra-small transistor patterns on a single chip [5] Perhaps more than any other process regime it is responsible for the phenomenal shrinkage of transistor circuitry over the past 30 years Although the end of cost effective photolithography has been predicted for many years, there is no obvious end in sight to our ability to continue to pattern state-of-the-art transistors using cheap photons Several years ago the first chip was made containing millions of transistors, the first billion-circuit chip is within our grasp, and a trillion-transistor chip is no longer something from the realm of science fiction

In photolithography a photoreactive organic film is deposited on the wafer, then exposed in precise regions using near-UV light It is common to find 250 nm photon sources, 220 nm will be implemented in manufacturing soon, and 193 nm ArF excimer light is currently in the research labs VUV and X-Ray sources have some significant hurdles to overcome before they are useful for manufacturing

The exposed regions are defined by a pattern mask, typically the mask has a magnification factor of at least 5 1, so that a 0 25 μm feature only requires a 1 25 μm feature on the mask Depending on the type of resist either the exposed or unexposed regions turn into highly insoluble features The soluble regions are removed from the wafer using a concentrated basic solution, leaving behind a wafer ready for pattern transfer

In generating a pattern it is actually easy to create a linewidth of 0 25 μm What is much more difficult is creating a space between lines of the same small dimension The pitch of lines is the sum of the space and linewidth Creating 0 25 μm lines on a 5 μm pitch is much easier than on a 0 5 μm pitch Perhaps even more challenging is creating a circular "hole" with a diameter of 0 25 μm Novel methods of laying down 0 01 μm wide metal lines are frequently touted as a significant advancement for the semiconductor industry, but until spaces and circles can be easily patterned these methods will not find their way into chip manufacturing

Anistropic plasma etching utilizes highly reactive species to remove macroscopic films from the water surface The directionality of the reactive ions will not attack the surface under regions coated with photoresist Thus after the plasma etch a permanent pattern remains in the film Following pattern etching the photoresist is no longer needed It is typically removed in an oxygen plasma, where organic species are converted to $CO_2$ and $H_2O$ Removal of the final 1% of the resist, and any inorganic species created in the pattern etching can be quite challenging, and this process spans the region between plasma etching and wafer cleaning In many cases the level of unwanted contaminant species must be lowered six orders of magnitude The first two are easy, the next two are harder, and the final two determine the difference between dead chips and profitability

Contamination removal is the area most in need of fundamental chemical understanding Microscopic chemical reactions at surfaces of planar wafers and sub-micron particles determine the efficacy of the process Frequently the phrase 'wafer cleaning' is used to describe these processes, however, removal of contamination is only a small component of the big picture In many cases actual etching determines the results and usually the final state of the wafer surface must be precisely controlled Thus the term surface preparation is more appropriate

Subsequent sections of this paper will focus on key areas where chemists can contribute significantly to our industry In many areas chemical understanding will aid us with superior processes with large cost savings, in some we simply want to understand what already works extremely well In all areas the phenomena are really interesting!

## 2 Surface Preparation

### 2.1 The RCA Standard Cleans and Piranha

In the late 1950s at RCA Laboratories Werner Kern and Norman Goldsmith were trying to remove sodium contamination from vacuum tubes [6] They found that concentrated acidic or basic peroxide solutions at 80 °C provided the cleaning power they were seeking As the semiconductor industry developed the need for powerful aqueous cleaning processes these two solutions were found to almost perfectly match its process requirements [7] Acronyms were to describe the steps Standard Clean 1 (SC1) for basic peroxide, and Standard Clean 2 (SC2) for acidic peroxide The initial decision on the concentration of these solutions was based on convenience, bottles of chemical with the 1 1 5 ratio were readily available (1 part 30% $H_2O_2$, 1 part either 37% HCl or 31% $NH_4OH$, and 5 parts $H_2O$) This ratio came to dominate the semiconductor industry, and it would be decades before the concentration and/or the temperature dependence of the process would be considered

The cleaning power of SC1 extends well beyond the semiconductor industry, it is used for such diverse applications as completely destroying skunk odour! This aqueous mixture of $NH_4OH$ and $H_2O_2$ is used to remove microscopic substances such as particles, organics, and inorganics, in addition to macroscopic films of oxide and metal SC1 is the primary particle/defect removal process used in manufacturing fabs [8] It etches $SiO_2$ and also Si (by forming an intermediate oxide surface film)

Lower concentrations of SC1 are now commonly used in modern wafer fabs [9] Significantly lowering the $NH_4OH$ concentration results in either no difference (thus cost savings) or superior performance (less pitting of exposed silicon surfaces) A high concentration of weakly acidic $H_2O_2$ coupled with very low hydroxide concentration leads to pH ranges well below those calculated by ignoring the dissociation of $H_2O_2$ And in concentrated $H_2O_2$ the solvation of $H^+$ and OH by $H_2O_2$ (instead of $H_2O$) should shift the water dissociation constant away from $1 \times 10^{14}$ New work is beginning to associate zeta-potential measurements with process performance, thus solution pH is becoming a critical variable for measurement and control [10] A quantitative understanding is required of pH, oxide etching, and wettability as a function of concentration and temperature to ensure these new solutions are fully optimized

Novel processing utilizing supersonic jets of cryogenic aerosols are being developed as a replacement for wet cleanings Argon is the current target for a process which can remove particulate and polymeric residue Particle removal is considered to be thermokinetic, the fast moving Ar snowball collides with a particle, transferring energy to the particle, breaking the surface 'bond' The move towards dry processing may someday eliminate the need for SC1 cleaning, but that day is probably well into the 21st century

Metal contamination can totally kill the electrical performance of

a transistor, so removing metals before a high temperature process drives them into the silicon is required. Most wafer processing tools are made of metal, thus stainless steel particles frequently deposit on the wafers. The SC2 solution is used nearly exclusively to remove metallic contamination. The hot acidic/oxidizing solution has worked well in the past. But for modern technology it adds far too many particles, and in fact has too much overkill. Recent studies have shown that a three order of magnitude decrease in HCl concentration shows virtually no impact, thus we can eliminate 99.9% of our acid costs without sacrificing anything.[11] In addition, this higher pH solution shows much lower particle deposition, thus it can actually increase our device yield.

Removal of organic contamination is accompanied by immersion in baths which deliver a large amount of reactive oxygen to the wafer. One frequently used reaction chemistry with extreme oxidizing power is commonly called a piranha solution. It is called piranha for obvious reasons, it reacts quite violently with skin! It is formed by mixing pure $H_2SO_4$ with 30% $H_2O_2$ in approximately a 4:1 ratio. Caro's acid ($H_2SO_5$) is assumed to be formed in high yield, and mixing concentrated acid with water raises the temperature. This solution can easily reach a temperature of 150 °C. It has been reported that the temperature spike is directly caused by metallic contamination, cleaner solutions have much lower peak temperatures. As the solution cools down to room temperature its ability to remove organic contamination from the wafer surface is degraded. The lifetime of the $H_2SO_5$ and the temperature dependence of its reaction with organic species need careful study. In addition, trace contamination such as Fe or other metals can catalyse decomposition of both $H_2O_2$ and $H_2SO_5$ so ultrapure solutions are required for this study. In modern facilities $H_2O_2$ is no longer used as the oxidant, rather $O_3$ is bubbled through a pure $H_2SO_4$ solution. This mixture must then be heated to 150 °C since it will not spontaneously heat to the required temperatures.

The true chemistry of SC1, SC2, and piranha solutions is an important aspect of the processes. Certain pseudo-chemical concepts are frequently bantered about; for example, 'a high concentration of both Cl and Cl* radicals in a hot SC2 solution' is commonly cited as the reason for the powerful cleaning capability. While the free radicals may indeed be present and crucial there is no data indicating either their presence in an acidic peroxide solution or their participation in the overall reaction chemistry. The available data support the theory that electrochemical oxidation–reduction reactions coupled with chemical oxidation ($H_2O_2$) dominate the chemical processes.

## 2.2 Particles and Defects

Most people know that particles kill chips, but the details are much more complicated. In most semiconductor companies particle sizes as small as 0.13 μm are routinely detected by laser scattering from crystal silicon surfaces. The ability of a particle this small to destroy a transistor is totally dependent on the exact time when the particle attacks the surface. A bare silicon wafer (first processing step) is nearly immune to such small particles, an exposed working transistor with polysilicon or metal conductors is the most sensitive. Particle composition varies almost as wildly. From skin/hair particles, to cotton, to stainless steel, to plastics . . . everything has the potential to generate yield killing defects.

In general the actual chemical identity of a particle or residue is unknown. Even if the elemental composition is known the bonding scheme defies current understanding. An example is a 0.15 μm diameter particle stuck at a critical point on a transistor. The total quantity of material contained within this particle is approximately 3 femtograms or about one million atoms. Knowledge of surface stoichiometry, internal bonding configurations, and even van der Waals attractive forces for an entity this small is quite challenging. While exact knowledge of these parameters would not immediately lead to an obvious removal procedure, it certainly would be an excellent starting point. Whether the material dissolves in a liquid, sublimates, or is physically dislodged from the surface is not particularly relevant. If any of these procedures works well then we will use it.

Removal of particles using liquids typically is accomplished with SC1. The solution is heated (40—80 °C) and/or agitated with sonic transducers (800 kHz). The actual chemistry and physics occurring at the surface during this process is fascinating, and not at all understood. Issues such as cavitation of dissolved gases, sonoluminescence, surface boundary layer effects, and wettability of the particles totally determine whether the process will remove 99% of existing particles, or less than 1%. A process which routinely removes 95% of known particles is considered excellent. It is interesting that the time dependence of particle removal seems to show that diffusion of the particles away from the surface is perhaps more important than the actual chemistry. Many instances are found where extended processing time significantly increases particle removal. The predominant mechanism appears to be re-deposition of particles which are not far enough from the surface during the water removal (drying) step.[12] As more particles get beyond the critical distance they do not deposit during drying.

Particle addition is much more dominant an issue in wafer processing, mainly because every single process step in the entire manufacturing line will add particles to a clean wafer. A good process will add less than 10 particles (> 0.15 μm) to a 200 mm diameter wafer, a poor process can add thousands. Particle removal processes are not an exception to this rule, clean wafers are frequently contaminated by 'cleaning' processes which remove 95% of the particles then add 200 more! Target defect densities are near one per chip after processing, which leads to the requirement of a single digit density per wafer for each individual process step.

The chemistry of particles is perhaps less important than physical effects. However, for removal of particles the solubility and wettability of the particle as a function of solution temperature and chemistry can totally determine the final percentage removed. Sticking energies rise significantly as the particle diameter decreases.[13]

The concept of a defect goes well beyond simple particles. A particle is a highly localized cluster of unacceptable atoms, but a defect can be almost completely delocalized. Figure 1 shows a scanning electron microscope (SEM) image of minor residue on both the top and sides of polysilicon lines. Removal of this residue is accomplished with a sequence of piranha followed by SC1.

The ability of an insulating $SiO_2$ film to survive high currents is directly related to the expected lifetime of a transistor. Accelerated lifetime testing is required to allow a guarantee of long life. Reliability of chip operation is the single most important aspect of manufacturing. It is easy to build a super-fast chip utilizing advanced technology. What is difficult is providing a guarantee that the chip will work for more than a few minutes. Typical reliability specifications are a 10 year lifetime while operated at 85 °C and 85% relative humidity.

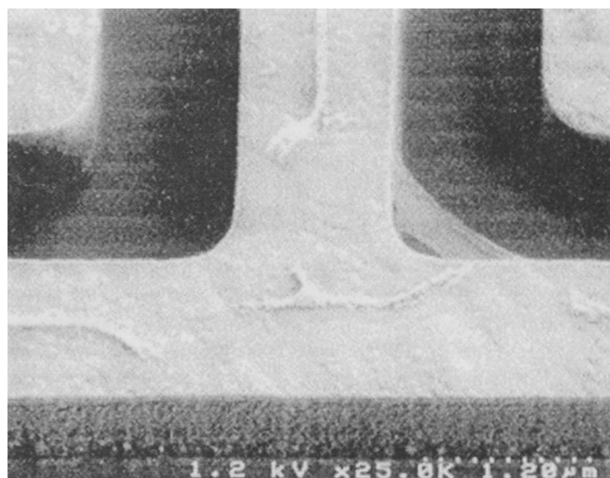



**Figure 1** SEM image of residue on top of polysilicon lines. Note the 'webbing' in the right-hand elbow. This residue will prevent transistor functionality if it is not removed, by either shorting adjacent lines or preventing electrical contact to metal leads.

For the transistor gate dielectric these extreme tests involve forcing milliamps of current through the 50 Å film, and waiting a few minutes for it to fail A good film can survive an integrated current density of 50 Coulombs $cm^{-2}$ before failure, while a poor film can explode after only 0 05 In addition to current, extreme voltage can destroy a film A good dielectric should hold off 10 MV per centimetre of thickness without significant leakage for hours In fact, for a high yielding wafer fab the failure of voltage breakdown testing should be less than 1 defect per 10 $cm^2$ of dielectric area (30 defects on a 200 mm wafer) A typical chip will have many orders of magnitude less area of active dielectric, and thus will never suffer dielectric failure

Failing these specifications is directly caused by chemical impurities If Fe or Al or Ca is present in large quantities on the wafer prior to gate dielectric growth, then that film will quickly fail the reliability testing It is only through the routine improvement in chemical purity that advanced microprocessors and DRAM chips can be made The purity of chemicals improves approximately an order of magnitude every 3 years A standard bottle of semiconductor grade $H_2O_2$ will now have less than 10 parts per trillion Fe contamination If this is never again improved, within 10 years transistor shrinkage will come to a dead stop

### 2.3 Wafer Drying

Wafers must be dried following wet processing This drying process can add particles, contaminants, and it can easily leave residue nearly identical with the 'waterspots' found on crystal glassware after dishwashing The challenge of drying a wet wafer is nearly as difficult as removing particles

Two primary techniques exist for drying Both are based on a fundamental concept '$H_2O$ should never evaporate from the wafer surface ' Evaporation of water can leave microscopic residue, even water which is ultraclean For example, a litre of ultrapure water can contain over 10 ppb total contamination After complete evaporation this equals as much as 10 $\mu$g of total contamination, enough to coat the entire wafer with a monolayer of deadly residue Since transistor feature sizes are near 0 25 μm, an evaporating droplet of water need only recede by 0 2—0 3 μm to leave enough residue to destroy a single transistor, which of course is enough to destroy the entire chip

The most common method of drying a wafer is by rapidly accelerating it to 2000 rpm, the centripetal acceleration coupled with high surface tension easily clears the wafer of all water With on-axis rotation the exact centre of the wafer actually does not move, and sometimes microscopic defects can be found at that spot Off-axis rotation at those speeds is much more challenging, heavy wafer loads must be precisely balanced to prevent wild shaking

The second method of wafer drying involves slightly modifying the effective surface tension of the liquid coating the wafer By lowering the surface tension either gravity or spinning or the Marangoni effect will leave behind a dry wafer The most common 'surfactant' used is isopropyl alcohol (IPA) IPA vapour will condense on a water film, and the resulting solution easily slides off a verticle wafer An IPA vapour dryer acts to transfer large quantities of heated IPA vapour to the water surface Dew point condensation of hot IPA onto the cooler wafers allows the IPA–water mixture to sheet off by gravity After a few minutes of condensation all water is gone, and only IPA coats the wafer Condensation raises the wafer temperature and after a few more minutes the wafers are hot enough that no more IPA can condense Marangoni drying is a modification of this effect Surface tension gradients in a IPA–water mixture at the wafer interface, allow a totally dry wafer to be extracted from the liquid

### 2.4 The Temperature Dependence of Wet Processing

A key variable frequently ignored in surface preparation is the temperature of the liquid Higher temperature can lead to superior performance, but the real chemistry is poorly understood A wide variety of thermodynamic and kinetic factors must be considered for full understanding such as solubility, surface tension and wettability, kinetic rates, diffusion, viscosity, and ionic concentration

Thermodynamic phenomena have a large impact Equilibria change with temperature and the solubility of many species increases as the temperature of the solvent is increased The ability of a solution to wet the wafer surface, and the surface tension of the liquid at the surface, can totally determine whether or not a particle is dissolved (or removed) The viscosity of a solution can strongly impact on the rate at which species can migrate towards or away from the surface Finally, the ionic concentration of pure water rises a factor of 20 as the temperature is raised from 25 to 80 °C Any reactions occurring in the final stages of rinsing could be accelerated by higher ionic content in hot water

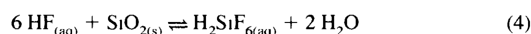
Kinetic phenomena also play a role Activation energies cause significantly higher reaction rates in hotter liquids The rate of diffusion of a species towards or away from the wafer increases with higher temperature Faster reactions are desirable because they allow more wafers to be processed per day even if there is no other technical reason for choosing a temperature

The temperature of piranha solutions is an interesting example of these issues It is not clear how much of the cleaning and oxidizing power is due to faster chemical reaction rates and how much results from other effects (increased solubility, diffusion rates, ionic concentration) By using ultraclean chemicals which reduce the peak temperature of the piranha, it is quite possible the process simply will not work While reducing chemical impurities is very important, this represents an example of why an uncontrolled reduction in impurities can be as devastating as a surprise increase

## 3 Isotropic Bulk Film Removal

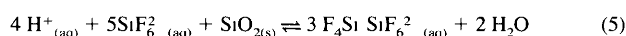
### 3.1 Silicon Dioxide Etching with Aqueous HF

The chemical reaction most widely used in this industry is removal of $SiO_2$ films using HF Mechanistic studies abound, however the influence of diffusion of reactants towards, and products away from, the surface has not been fully understood Indeed the overall chemical reaction remains in dispute Common wisdom identifies (4) as the primary reaction in liquids



$$6\,HF_{(aq)} + SiO_{2(s)} \rightleftharpoons H_2SiF_{6(aq)} + 2\,H_2O \qquad (4)$$

However, more than 40 years ago the product $H_2SiF_6$ species was found to easily attack $SiO_2$ as shown in eqn (5) [14]



$$4\,H^+_{(aq)} + 5SiF_6^{2-}{}_{(aq)} + SiO_{2(s)} \rightleftharpoons 3\,F_4Si\;SiF_6^{2-}{}_{(aq)} + 2\,H_2O \qquad (5)$$

From a mechanistic standpoint (5) may be critical to a complete understanding of the process because when (4) is complete the $H_2SiF_6$ species is formed within a few Å of the wafer surface Thus virtually no migration of reactants towards the $SiO_2$ would be required to initiate reaction (5) Only steric hindrance, rotational orientation, and solvent cage effects will prevent nearly instaneous reaction In fact it may be impossible to separate the effects of the two reactions

The rate at which $SiO_2$ is removed from a wafer surface strongly depends on such factors as the concentration of HF and the pH of the solution (using $NH_4F$ as a buffer) It has long been known that the etch rate increases as $NH_4F$ is added to an HF solution But near 15 mass% it peaks and decreases with further buffering Recent work has shown that this is not only true when the HF mass% is constant, but also when it changes during water dilution as shown in Figure 2 [15]

The actual chemistry of this not only depends on the liquid, but also strongly depends on the exact form of the $SiO_2$ which is being removed Thermally grown oxide films etch the slowest, while deposited films (TEOS) and highly doped boron–phosphorus silicate (BPSG) glasses have very different behaviour

A debate currently is in progress surrounding this data One theory involves the surface sites where reactant species attack the $SiO_2$ [16] As the solution becomes extremely rich in inert $NH_4^+$

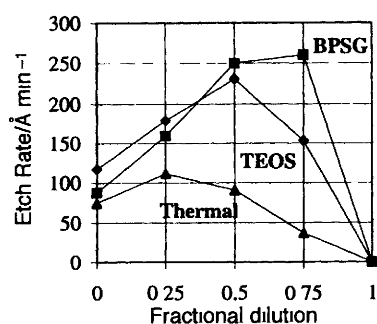



**Figure 2** Etch rate of deposited (either TEOS or BPSG) and thermally grown $SiO_2$ films as a function of water dilution of 0 49 mass% HF + 40 mass% $NH_4F$ As more water is added (moving left to right) the etch rate increases, despite the fact that the total HF concentration is also dropping It is not until nearly 80% dilution that the etch rate begins to approach zero

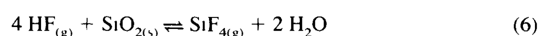
species they block the surface from attack by reactant $HF_2^-$ The other involves the diffusion of reactants towards and of products away from the surface [15] In this theory the measured rate moves from being diffusion limited for concentrated solutions to chemial reaction rate limited in dilute liquids Mechanistic chemistry studies are needed to fully analyse the etching dynamics of this system and determine the relative contributions of steric/site hindrance and diffusion

### 3.2 Silicon Dioxide Etching with Gas Phase HF

Gas phase reaction chemistry is becoming significantly more important to our industry This is driven by three key factors cost reduction, waste disposal and safety Gases tend to be significantly less expensive than ultrapure liquid chemicals Not only is the cost of procuring a chemical important, the cost of disposal frequently exceeds the purchase price[1] Water, the simplest chemical in the industry, can represent drastic expenditures in such localities as Albequerque or Singapore Use of gas phase processing in many cases is far more economical

Environmental concerns drive the goal of reduction of chemical waste disposal In many cases elimination of such chemicals as chlorofluorocarbons, global warmers and carcinogens are motivated by more important issues than disposal Finally, safety can be a key issue Aqueous HF is a highly insidious chemical, dangerous exposures can go undetected for hours

Thus the gas phase reaction between $SiO_2$ and HF is receiving intense development as a replacement for wet processing Recent work has attempted to discern the fundamental processes including condensation, evaporation, and chemical reactions [17] Volatile $SiF_4$ is assumed to be the primary product in a variation of (4), eqn (6)



$$4\,HF_{(g)} + SiO_{2(s)} \rightleftharpoons SiF_{4(g)} + 2\,H_2O \quad (6)$$

However this reaction cannot self-initiate A hydrogen containing solvent species is required as a reactant, either $H_2O$, an alcohol, or acetone can be used Whether the hydrogen species is catalytic or a true reactant, if it solvates intermediate products, and/or acts to raise the vapour pressure of products is almost totally unknown at this time HF reacting with $SiO_2$ yields water, thus this process can be self-perpetuating after the initial surface reaction occurs

The dynamics of this etch process are convoluted, with a 'negative' activation energy dominating the reactions [18] The decrease in effective etch rate with increasing temperature is of course not a decrease in the true chemical reaction rate Rather the overall process is the sum of several competing processes, one of which is desorption of the adsorbed alcohol molecules It appears that des orption limits the overall rate by removing the reactant hydrogen species Thus even though the chemical reactions are much faster at elevated temperatures, the overall etch rate decreases by an order of magnitude when the temperature is increased from 45 to 90 °C Since the alcohol is not required for perpetuating the reaction perhaps it simply forms a complex with a product species, aiding in evaporation

Implementation of dry etching into manufacturing fabs is certainly many years away The wet process works so well that a very good reason must be found to switch to such an experimental technique As described above, the potential advantages are significant, however, to date the process is neither stable enough nor obviously superior

### 3.3 Silicon Nitride Etching with $H_3PO_4$ and Fluorine Atoms

In many cases a nitride film is used, for a specific patterning sequence, but then the film is no longer needed and the chip will not function unless this sacrificial film is removed Its removal requires a reasonably fast rate of removal of nitride, with almost no simultaneous removal of oxide In fact, removal of oxide can be disastrous under certain circumstances In 1967 the first paper was published on the use of $H_3PO_4$ for selective removal of $Si_3N_4$ with respect to $SiO_2$ [19] This process is for all practical purposes identical with that planned for use in all chip manufacturing through at least the year 2000 The water content of the heated acid solution strongly impacts the etch rate of $SiO_2$ In addition, the silicon content of the bath also strongly influences the $SiO_2$ etch rate The mechanism is assumed to be hydrolysis of the nitride film to solvated $SiO_2$ and $NH_3$ but again the true chemistry is not well understood

Elimination of wet chemical nitride etching is being studied using F radical processes The potential for superior process uniformity, etch rate control, cost savings, and chemical disposal all point to chemical dry etching as an obvious replacement for $H_3PO_4$ Many companies are now studying preliminary processing tools, as a prelude to implementation into full manufacturing But once again, until specific advantages are found no change will be made

### 3.4 Titanium Nitride Etching with $H_2O_2$

The resistivity of Si films is too high to support the ultrafast processing speeds required for modern transistors Strapping the line with a low resistivity material solves this, but of course adds several new problems The most common strap material is $TiSi_2$ The self-aligned silicide process involves depositing titanium on a wafer having exposed Si and $SiO_2$ films [20] Subsequent thermal processing (near 575 °C in $N_2$) effects formation of the C49 phase of $TiSi_2$ in regions on the wafer where the Ti is in contact with Si C49 is the high resistivity crystalline form of $TiSi_2$ Where the Ti contacts $SiO_2$ the $N_2$ 'burns' the titanium into titanium nitride After $TiSi_2$ formation the TiN and any unreacted Ti must be removed leaving behind the electrical leads for the transistors After removal the $TiSi_2$ is annealed to the low resistivity C54 phase

Removal of TiN recently became a crucial issue, mainly because the wet etch solution was poorly characterized Luckily the process was more than adequate for the 1980s and thus the poor under standing of concentration and pH dependence did not limit us However, in the 1990s the thickness of these critical films is decreasing to levels which can no longer tolerate non-optimized processing

Removal of the TiN is actually quite facile, the problem is that the thickness of the $TiSi_2$ is critical, as much as possible must remain after the TiN removal An insidious twist is that a small frac tion of the $TiSi_2$ must be removed, otherwise important transistors may be shorted Previous work has focused on the piranha and SC1 solutions as etchants The relative etch rates of $TiSi_2$ and TiN deter mine the success or failure of the process As seen in Table 1 the selectivity changes drastically over a range of easily accessible SC1 concentrations and temperatures [21] The process ratios are for volumes of 30% $H_2O_2$, 30% $NH_4OH$, and water

Understanding the etch mechanism of both films would greatly improve this process The etching of TiN is varies drastically as the $NH_4OH$ and $H_2O_2$ concentrations are changed as shown in Figure 3 Obviously electrochemistry plays a key role, because electrochemical oxidation of titanium is required The exact role of the $H_2O_2$ and OH species, the fate of the nitrogen atoms, the true

**Table 1** Etch rates (ER) for salicide strip

| Process $NH_4OH:H_2O_2:H_2O$ | $T$/°C | TiN ER /Å $min^{-1}$ | $TiSi_2$ ER /Å $min^{-1}$ | Selectivity |
|---|---|---|---|---|
| 1:1:6 | 27 | 57 | 7.3 | 7.8 |
| 1:200:600 | 27 | 35 | 3.1 | 11 |
| 1:200:600 | 55 | 130 | 11.8 | 11 |
| 1:200:0 | 40 | 67 | 4.0 | 17 |
| 1:200:0 | 55 | 280 | 13.9 | 20 |
| 0:1:0 | 55 | 120 | 2.3 | 52 |

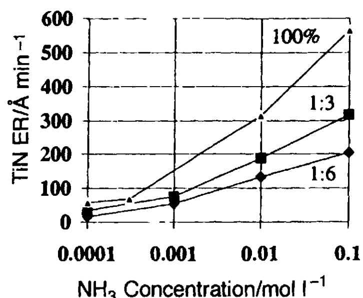



**Figure 3** Etch rate of TiN (Å $min^{-1}$) in various solutions of $H_2O_2$ and $NH_4OH$. The ammonia concentration at 0.0001 $mol^{-1}$ is actually zero (for convenience). The $H_2O_2$:$H_2O$ ratio varies as 1:6, 1:3, or 1:0 (= straight 30% $H_2O_2$).

reaction leading to dissolution of TiSi2 . . . all of these unknowns are important to fully optimize this process.

After several $\mu$g of TiN have been dissolved in $H_2O_2$ a deep yellow or orange solution is formed. The colour and the long term stability indicate that a coordination complex between Ti cations and peroxide anions is formed. While familiar to many inorganic chemists this reaction comes as a complete surprise to the semiconductor industry. The conventional wisdom is that metal impurities act as catalysts for the decomposition of $H_2O_2$.[22] In fact, it is only since 1990 that unstabilized 30% $H_2O_2$ is clean enough that it will last weeks without significant decomposition. The decomposition of an etching solution costs money (because the lost $H_2O_2$ must be replaced) and is easily observed for Fe contamination. The long term stability of the Ti–$H_2O_2$ solution is a novel result. Understanding the stability of the Ti–$H_2O_2$ solution as a function of temperature and concentration will lead to minimizing chemical usage and expenses.

## 4 Metallization

### 4.1 The Metal Stack

Metal conductors on semiconductor chips need to have the lowest resistance possible, to minimize the RC (resistance–capacitance) time delay for signal propogation. Modern microprocessors requiring 200 MHz operation cannot utilize tungsten or TiW alloys, aluminium is required. However, Al can diffuse through the underlying film, and it cannot be patterned properly due to the high reflectivity. Thus the metal conductor stack is a thin layer of titanium nitride, on top of a thick layer of Al, on top of a diffusion barrier (another thin layer of TiN), as shown in Figure 4.

Electromigration is the physical transport of bulk metal under an applied electric field. The effects of electromigration prevent the use of pure Al, so a 0.5% Cu alloy used. At some point (unless room temperature superconductors are found) the most poisonous contaminant in our industry, Au, will be required for super-fast chip speeds. Au diffuses through silicon easily, and acts to kill transistor switching.

Because of the lack of ability to lower R, lowering C has become a critical issue. Low relative permittivity insulators capable of

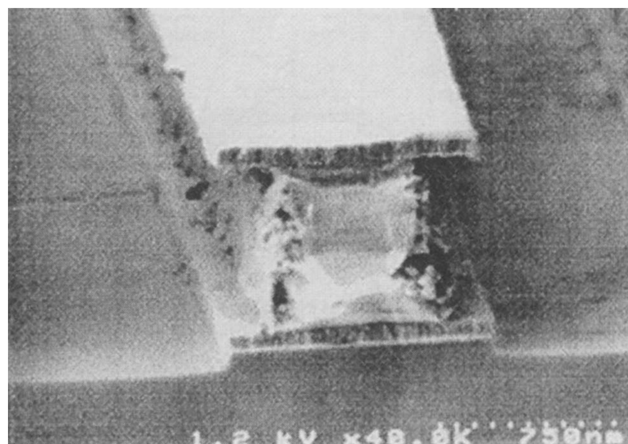


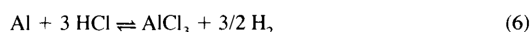
**Figure 4** An SEM cross section of a typical metal line. The TiN layers are seen on top of, and beneath the Al. At the sidewall some of the Al has been removed during the etch and clean steps. This loss of Al degrades the electrical conductivity of the line.

implementation into chip manufacturing are desperately needed. Teflon, parylene, other fluoropolymers, xerogels, and porous silicon are all under intensive study to determine their physical characteristics.

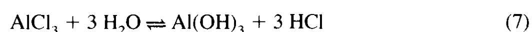
### 4.2 Corrosion

The corrosion of aluminium is an issue which costs human society billions of dollars. The corrosion of aluminium electrical lines costs the semiconductor industry millions of dollars every year. Some portion of the net cost of a chip is associated with preventing the electrical conductors from corroding so we can guarantee that the chip will work for 10–20 years after it is sold. Aluminium is highly reactive to exposure to moist air, $Al_2O_3$ is formed nearly instantaneously. Luckily this dense coating serves as a barrier to air, preventing further reaction, and a piece of aluminium is extremely stable unless exposed to a corrosion catalyst.

Catalytic corrosion of aluminium by chlorine involves the reaction pair (6) and (7).



$$Al + 3\,HCl \rightleftharpoons AlCl_3 + 3/2\,H_2 \quad (6)$$

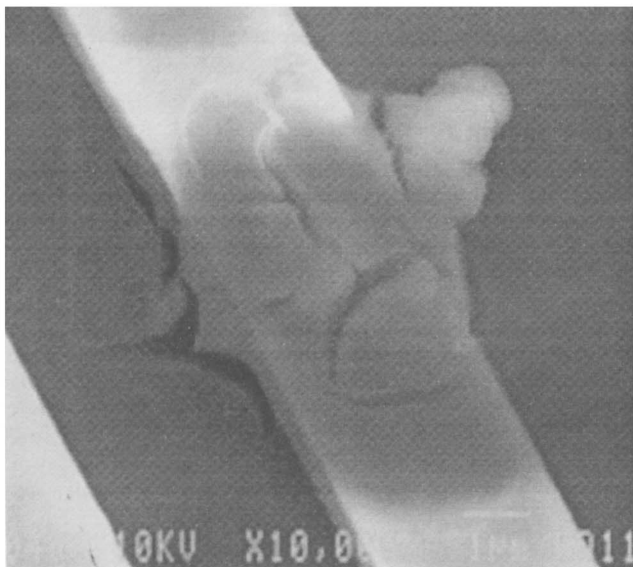


$$AlCl_3 + 3\,H_2O \rightleftharpoons Al(OH)_3 + 3\,HCl \quad (7)$$

Ambient oxygen and moisture serve to reduce Al at the metal surface creating a corrosion barrier, but the chlorine forms $AlCl_3$ which is easily transported through the passivating film from a pit near the metal–oxide interface to the oxide–air interface. Corrosion is accelerated at Al–Cu grain boundaries, so the need to add Cu for electromigration resistance is balanced by its detrimental impact on corrosion.

Unfortunately plasma etching of aluminium is dominated by chlorine species, and it is only through an intense sequence of exposure to water and other chlorine removing chemicals that the aluminium survives. It is unproved whether or not Cl is the primary contaminant causing corrosion. There is no question that poor removal of chlorinated residue results in severe corrosion. What is more uncertain is whether or not minor corrosion on otherwise good wafers is due to Cl.

Corrosion of Al is caused by virtually every anionic species.[23] Elimination of all carbonate, nitrate, sulfate, fluoride species from cleanroom air is nearly impossible. In fact, cleanroom air is not filtered for molecule sized contaminants. Only particles larger than 0.1 $\mu$m are removed. There is no current way to prove beyond a doubt what causes corrosion of aluminium electrical lines. While hundreds of laboratories are studing the passivation of metal surfaces, this topic needs much more extensive development. A key point for the semiconductor industry is that a typical passivating film can be several hundreds of Angstroms thick. But since metal



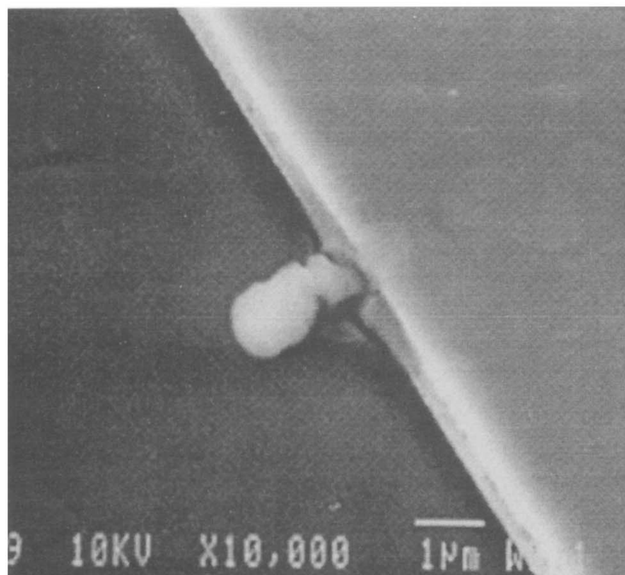
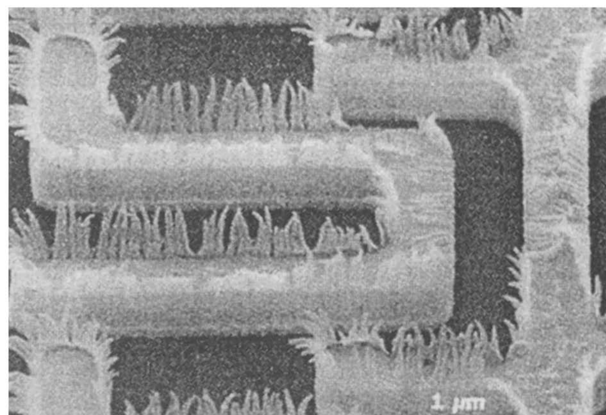


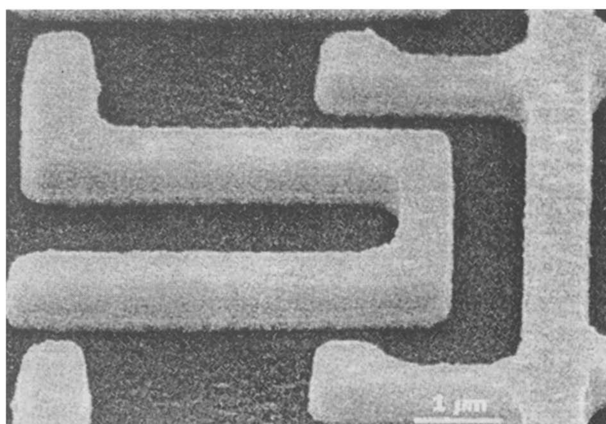

**Figure 5** Corrosion of aluminium. the volumetric expansion in converting Al to $Al_2O_3$ pushes upwards, and cracks through the TiN coating layer (top). Since the top of the Al is covered, corrosion usually is seen as originating on the sidewalls (bottom).

lines are only 3500 Å wide (and plummeting) a thick passivating layer consumes too much of the precious metal conductor, and the final electrical resistance of the line would be too high. Alternatively, covering the line with a thick coating (*i.e.* paint) would consume too much of the space between lines, which is required for electrical isolation. Generating a passivating aluminium coating which is only 10—20 Å thick would greatly benefit our industry.

### 4.3 Polymer Removal

The plasma etching which forms small metal line features (less than 0.5 μm wide) requires a passivation technique to result in flat sidewalls which are perpendicular to the wafer surface. A taper (either positive or negative) results in unacceptable electrical performance. In order to achieve this sharp profile and maintain tight control over linewidth a technique is used which deposits a fluorocarbon polymer on the exposed sidewall during the plasma etch process. The stoichiometry of this film is not well characterized, but in




removal without destroying the metal lines is difficult. Frequently it requires use of solvents such as dimethylacetamide, or *N*-methylpyrrolidinone, followed by IPA rinsing. Removal of the sidewall polymer has recently been advanced, by the use of vapour HF technology (described above).[24] Figure 6 shows the impact of vapour HF on the polymer.

## 5 Metrology

### 5.1 Trace Contaminant Detection

Ultra-sensitive analytical techniques are required to allow our industry to maintain the purity of liquid chemicals required for functional devices. In a typical SC1 process tank the sum total of all metallic impurities should be well under 10 ppb. Individual elemental impurities should be below 1 ppb. Detection of these species is challenging, not only from the analysis itself, but also from the sample collection procedure. A clearly defined and controlled protocol is required to guarantee that the final impurity concentration is truly from the sample, and not from the collection bottle or technician.

Inductively coupled plasma mass spectrometry (ICP-MS) is the standard contaminant analysis technique used for most liquid samples. In some cases the ppb sensitivity of ICP-MS is not sufficient, and graphite furnace atomic absorption spectrometry (GFAA) is used. In combination we have the ability to verify on a routine basis that no single contaminant is above 0.5 ppb. An alternative technique on the rise is capillary electrophoresis.

Improvements in sensitivity must obviously continue in these types of analysis as transistors become smaller. It appears that we

can tolerate the status quo for 3–5 more years, but certainly by the 21st century we will need routine sensitivity of 50 ppt for contaminants such as Fe and Na In addition to the most common liquid (water), analysis of the viscous acids $H_2SO_4$ and $H_3PO_4$ will be required at these extreme levels Currently ICP-MS and GFAA cannot supply the trace sensitivity for these viscous chemicals

The current standard for analysing surface impurities is total reflection X-ray fluorescence (TRXRF) Although limited to elemental analysis, the routine detection limit below $10^{10}$ atoms per $cm^2$ is comparable to the required cleanliness of our surfaces Extending this technique to better sensitivity will probably require bright X-ray sources such as found in a synchrotron Time-of-flight secondary ion mass spectrometry (TOF-SIMS) and traditional SIMS are currently under development for quantitative surface analysis These techniques offer the tremendous potential of molecular analysis, however, an accuracy near $\pm$ 20% is required before any technique is useful for us

### 5.2 Statistical Process Control

The evolution from academic research to pure manufacturing is best described as an increase in the repeatability of the action Whether it is patterning, or etching, or deposition, a graduate student research project is considered completed after it has worked well three or four times The more typical situation is the near daily failures of laser alignment, computer crashes, a dead resistor or vacuum failures

In manufacturing a mature process must work perfectly close to 1 million times in a row Profitability is completely lacking in a set of procedures which only works 1000 times in a row before failing In a modern DRAM chip a single pattern step will generate 64 million features, if any one of these fails the entire chip is useless The industry is very quickly moving towards the goal of ppb failure rates on individual processes Motorola's 6-sigma program (and comparable programs at most semiconductor companies) are driving towards reducing the standard deviation of a process to 1/12th of the specification range Thus if a film can be between 100 and 112 Å thick, then the 6-sigma goal is 106 $\pm$ 1 0 Å (one standard deviation) This results in a failure rate of 2 parts in $10^9$ (for a normal distribution)

A good example is the construction of a video camcorder A typical recorder will have about 1000 parts If the failure rate of each of these individual parts is 1/999 then the overall failure rate of all final products is *ca* 63% This is calculated almost exactly as the yield of an overall organic synthesis, eqn (8)

$$Y = (1 - 1/999)^{1000} \quad (8)$$

Every chemist knows that the overall yield of a multi-step reaction sequence can be quite small, even if each individual reaction has 90% yield It is difficult to imagine a company making any profit off a product line where only 37% of the manufactured devices function properly Using eqn (8) it is easy to see that 90% overall success on manufactured camcorders requires a failure rate for individual parts of well below 1 ppm

The use of statistical process control has been described as the single most important reason for the incredible success of the Japanese industrial base Most semiconductor companies throughout the world have now embraced the principles of Deming and Juran, with obviously successful results [25,26] The concept of ppm failure rates is certainly out of the realm of academic research, but it helps researchers to understand why some fantastic academic advances are nearly useless to our industry If the new idea is not reproducible enough then we will probably never be able to make any profit from it

## 6 Conclusions

The overwhelming success of the semiconductor industry over the past 30 years is strongly dependent on chemical reactions Despite its success our industry has a poor understanding of the detailed physical and inorganic chemical reactions and principles upon which its key processes are based Professional chemists have a significant opportunity to contribute key information which can either reduce the costs of currently produced integrated circuits, or enable the future production of new technology (smaller transistor) chips

In wet etching using HF, $H_3PO_4$, acidic or basic peroxide the true chemical mechanisms are almost totally unknown In microscopic contaminant removal the situation is even worse because the true chemical identity of the target species is also unknown Fundamental chemical research will greatly aid in tailoring a specific chemical reaction to attack a specific species

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